Remarks

Applicants respectfully request reconsideration of this application as amended. Claims 1 and 11 have been amended. No claims have been cancelled. Therefore, claims 1, 4-11, 13-22, 24 and 26-28 are presented for examination.

Claims 1-10, 18-22, 24, and 26-28 stand rejected under 35 U.S.C. §102(b) as being anticipated by Jenkins, IV (U.S. Patent No. 6,184,708). Applicants submit that the present claims are patentable over Jenkins.

Jenkins discloses input/output blocks (IOBs) each including an I/O pad, tri-state output buffer, input buffer, and slew rate control circuit, among other components. The I/O pad is connected to a trace of a printed circuit board. The output terminal of the output buffer is connected to the I/O pad. The output buffer is a tri-state buffer which is controlled by the slew rate control circuit and a tri-state control circuit. The tri-state control circuit controls the output buffer 211 to be in an enabled state or a high-impedance state. The slew rate control circuit controls the rate at which the output signals provided by the output buffer change value. The slew rate control circuit is programmable to provide a plurality of pre-determined slew rates. Configuration memory cells associated with slew rate control circuit are programmed to store configuration data values which define the slew rate of slew rate control circuit. During the slew rate test, a configuration processor programs these configuration memory cells to store the desired configuration data values, thereby causing slew rate control circuit to provide the desired slew rate. See Jenkins at Figure 3 and col. 4, ll. 66 – col. 5, ll. 40.

Claim 1 of the present application recites a slew rate detection mechanism to receive an output signal transmitted from an I/O buffer, to detect a slew rate of the output signal and

to generate a signal indicating a status of the slew rate. Applicants submit that nowhere in Jenkins is there disclosed a slew rate detection mechanism that detects a slew rate received from an output signal and generates a signal indicating a status of the slew rate. Instead, Jenkins discloses a slew rate control circuit is programmable that provides a pre-determined slew rate based on stored configuration data values. During a slew rate test, a configuration processor programs causes the slew rate control circuit to provide a desired slew rate based on a stored value. Applicants submit that a control circuit that is programmed to provide a pre-determined slew rate **cannot be considered as anticipating *a slew rate detection mechanism that detects a slew rate of a received output signal and generates a signal indicating a status of the slew rate.*** Therefore, claim 1 is patentable over Jenkins. Claims 4-10 depend from claim 1 and include additional features. Therefore, claims 4-10 are also patentable over Jenkins.

Claim 18 recites receiving a signal at a slew rate detection mechanism within a chipset via a bus and generating a signal indicating the status of the slew rate. For the reasons described above with respect to claim 1, claim 18 is also patentable over Jenkins. Since claims 19-21 depend from claim 18 and include additional features, claims 19-21 are also patentable over Jenkins.

Claims 11 and 13-17 stand rejected under 35 U.S.C. §102(b) as being anticipated by Chen et al. (U.S. Patent No. 6,477,592). Applicants submit that the present claims are patentable over Chen.

Chen discloses a memory controller including a CDS output buffer circuit provided for data transmission signals output to and received from, for example, one or more memory

modules. The CDS output buffer circuit includes a data encoder circuit, a slew rate control circuit, and an output driver circuit. See Chen at Figure 5.

Claim 11 of the present application recites a slew rate detection mechanism to receive an output signal transmitted from an I/O buffer, to detect a slew rate of the output signal and to generate a signal indicating a status of the slew rate. Applicants submit that Chen fails to disclose such a mechanism. Instead, Chen disclose a slew rate control within an output buffer that does not disclose detecting a slew rate of a received output signal and generating a signal indicating a status of the slew rate. Therefore, claim 1 is patentable over Chen. Because claims 24 and 26-28 depend from claim 22 and include additional features. Therefore, claims 24 and 26-28 are also patentable over Chen.

Applicants respectfully submit that the rejections have been overcome and that the claims are in condition for allowance. Accordingly, applicants respectfully request the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

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